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EXAMINER	
THAMMAVONG, PRASITH	

ART UNIT	PAPER NUMBER
2187	

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12/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,330	WOLRICH ET AL.	
	Examiner	Art Unit	
	PRASITH THAMMAVONG	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action reopens prosecution as noted by the Notice of Panel Decision from Pre-Appeal Brief Review dated 10/19/2009.

The instant application having Application No. 10/780,330 has a total of 18 claims pending in the application, there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

1. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 28-30, 32 and 34-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Sharma (US Patent # 6,055,605).

With respect to claim 28, the Tremblay reference teaches a processor, comprising:

multiple programmable units integrated within the processor; (fig. 3, element 306 and column 4, lines 7-29, where the registers are within the processors)

logic integrated within the processor to map resources within the multiple programmable units into a single address space, (column 4, lines 7-29, where the registers are mapped collectively to a address space in the instruction cache 212) and

wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specified in an instruction and the registers in P1 processor 208)

However, the Tremblay reference does not explicitly teach that the logic is to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space.

The Sharma reference teaches that is conventional to have the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space. (see fig. 1, and column 6, lines 8-15, where there is a shared memory with a single address space shared by a plurality of processors; and column 4, lines 8-39, where each processor has their own private cache for storing data and changes to the data as a result of the memory reference operations are reflected among the entities

via the transmission of probe commands in accordance with a conventional cache coherence protocol and where the ordering point requests forwarding of the data from the owner processor to the requesting processor, as required by the memory operation)

The Tremblay and Sharma references are considered analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify the Tremblay reference to have the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, as taught by the Sharma reference.

The suggestion/motivation for doing so would have been to improve performance of the multiprocessor system by reducing the latency of inter-reference ordering. (Sharma, column 3, lines 46-60)

Therefore, it would have been obvious to combine the teachings of Tremblay reference with the Sharma reference for the benefit of improving performance as specified in claim 28.

With respect to claim 29, the combination of the Tremblay and Sharma references teaches the processor of claim 28, wherein the resources within the multiple programmable units comprise register locations within the multiple programmable units.

(Tremblay, column 4, lines 7-29, where the registers are programmed with address information)

With respect to claim 30, the combination of the Tremblay and Sharma references teaches the processor of claim 28, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable units. (Tremblay, column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

With respect to claim 32, the combination of the Tremblay and Sharma references teaches the processor of claim 28, wherein the multiple programmable units comprise multiple programmable multi-threaded units. (Tremblay, column 6, lines 14-45, where the registers can have multi-threaded instructions within them)

With respect to claim 34, the combination of the Tremblay and Sharma references teaches the processor of claim 28, wherein the logic comprises logic to receive a command from a programmable processor. (Tremblay, column 4, lines 7-29, where P2 processor 210 can issue commands as well)

With respect to claim 35, the combination of the Tremblay and Sharma references teaches the processor of claim 34, wherein the multiple programmable units comprise multiple programmable engines and the programmable processor. (Tremblay, column 4, lines 7-29, where P2 processor 208 can issue commands as well and where there is registers within the P2 processor 210)

With respect to claim 36, the Tremblay reference teaches a method, comprising:

mapping addresses in a single address space to resources within a set of multiple programmable units integrated within a processor, the single address space including addresses for different ones of the resources in different ones of the multiple programmable units; (column 4, lines 30-58, where there is one-to-one correlation between the registers specified in the instruction and the registers in P1 processor 208) and

wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specifies in an instruction and the registers in P1 processor 208)

However, the Tremblay reference does not explicitly teach providing data access to a resource within a first of the multiple programmable units to a second one of the

multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space.

The Sharma reference teaches that is conventional to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space. (see fig. 1, and column 6, lines 8-15, where there is a shared memory with a single address space shared by a plurality of processors; and column 4, lines 8-39, where each processor has their own private cache for storing data and changes to the data as a result of the memory reference operations are reflected among the entities via the transmission of probe commands in accordance with a conventional cache coherence protocol and where the ordering point requests forwarding of the data from the owner processor to the requesting processor, as required by the memory operation)

The Tremblay and Sharma references are considered analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify the Tremblay reference to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, as taught by the Sharma reference.

The suggestion/motivation for doing so would have been to improve performance of the multiprocessor system by reducing the latency of inter-reference ordering. (Sharma, column 3, lines 46-60)

Therefore, it would have been obvious to combine the teachings of Tremblay reference with the Sharma reference for the benefit of improving performance as specified in claim 36.

With respect to claim 37, the combination of the Tremblay and Sharma references teaches the method of claim 36, further comprising receiving a command specifying the address in the single address space. (Tremblay, column 4, lines 7-29, where the registers are mapped collectively to a address space)

With respect to claim 38, the combination of the Tremblay and Sharma references teaches the method of claim 37, wherein the command comprises one selected from the following group: a read command and a write command. (Tremblay, column 7, lines 8-33, where the information is read from and stored into the registers)

With respect to claim 39, the combination of the Tremblay and Sharma references teaches the method of claim 37, wherein the receiving the command

comprises receiving the command from a programmable processor. (Tremblay, column 4, lines 7-29, where P2 processor 210 can issue commands as well)

With respect to claim 40, the combination of the Tremblay and Sharma references teaches the method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor; and wherein the multiple programmable units comprise multiple programmable engines and the programmable processor. (Tremblay, column 4, lines 7-29, where P2 processor 208 can issue commands as well and where there is registers within the P2 processor 210)

With respect to claim 41, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the resources within the set of multiple programmable units comprises register locations within the multiple programmable units. (Tremblay, column 4, lines 7-29, where the registers are programmed with address information)

With respect to claim 42, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the single address space comprises addresses corresponding to shared resources external to the multiple

programmable units. (Tremblay, column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

With respect to claim 43, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the multiple programmable units comprise multiple programmable multi-threaded units. (Tremblay, column 6, lines 14-45, where the registers can have multi-threaded instructions within them)

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Sharma (US Patent # 6,055,605) as applied to claim 28 above, and further in view of Tran (US Patent # 6,138,240).

With respect to claim 31, the combination of the Tremblay and Sharma references teaches the processor of claim 30, wherein the shared resources external to the multiple programmable units comprise a memory internal to the processor and a randomly accessible memory external to the processor. (Tremblay, fig. 3, element 306 and 202; and column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

However, the combination of the Tremblay and Sharma references does not explicitly teach a Peripheral Component Interconnect (PCI) unit.

The Tran reference does teach that is conventional to have a Peripheral Component Interconnect (PCI) unit. (column 4, lines 37-49)

The Tremblay, Sharma and Short references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Tremblay and Sharma references to have a Peripheral Component Interconnect (PCI) unit, which is taught by the Tran reference.

The suggestion/motivation for doing so would have been to allow high speed access for peripherals. (Tran, column 4, lines 37-49)

Therefore it would have been obvious to combine the teachings of the Tremblay and Sharma references with the Tran reference for the benefit of high speed access to obtain the invention as specified in claim 31.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Sharma (US Patent # 6,055,605) as applied to claim 28 above, and further in view of Short (US Patent # 5,633,865).

With respect to claim 33, the combination of the Tremblay and Sharma references does not explicitly teach there is an interface to a media access controller (MAC).

The Short reference does teach that is conventional to have an interface to a media access controller (MAC). (column 3, lines 4-31)

The Tremblay, Sharma and Short references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Tremblay and Sharma references to have an interface to a media access controller (MAC), which is taught by the Short reference.

The suggestion/motivation for doing so would have been to allow access to networks via the MAC (column 3, lines 4-31).

Therefore it would have been obvious to combine the teachings of the Tremblay and the Sharma references with the Short reference for the benefit of network access to obtain the invention as specified in claim 33.

Claim 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Short (US Patent # 5,633,865) and Sharma (US Patent # 6,055,605).

With respect to claim 44, the Tremblay reference teaches a device, comprising:

at least one processor, (see fig. 3, elements 208 and 210) the processor comprising:

multiple programmable units; (column 6, lines 14-45, where the registers can have multi-threaded instructions within them) and

logic to map resources within the multiple programmable units and resources external to the multiple programmable units into a single address space, the resources within the multiple programmable units comprising register locations, (column 4, lines 7-29, where the registers are mapped collectively to an address space) the resources external to the multiple programmable units comprising at least one Random Access Memory (RAM) external to the processor, (column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory) and

wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specifies in an instruction and the registers in P1 processor 208)

However, the Tremblay reference does not explicitly teach that there is at least one media access controller (MAC) coupled to the at least one processor; and the logic is to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, (column 4, lines 7-29, where the instruction cache allows the processors to access data within the registers of the processors)

The Short reference does teach that it is conventional to have there be at least one media access controller (MAC) coupled to the at least one processor. (column 3, lines 4-31)

The Tremblay and Short references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Tremblay reference to have at least one media access controller (MAC) coupled to the at least one processor, which is taught by the Short reference.

The suggestion/motivation for doing so would have been to allow access to networks via the MAC (column 3, lines 4-31).

However, the combination of Tremblay and Short references does not explicitly teach that the logic is to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space.

The Sharma reference teaches that is conventional to have the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space. (see fig. 1, and column 6, lines 8-15, where there is a shared memory with a single address space shared by a plurality of processors; and column 4, lines 8-

39, where each processor has their own private cache for storing data and changes to the data as a result of the memory reference operations are reflected among the entities via the transmission of probe commands in accordance with a conventional cache coherence protocol and where the ordering point requests forwarding of the data from the owner processor to the requesting processor, as required by the memory operation)

The Tremblay, Short and Sharma references are considered analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify the combination of the Tremblay and Short references to have the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, as taught by the Sharma reference.

The suggestion/motivation for doing so would have been to improve performance of the multiprocessor system by reducing the latency of inter-reference ordering. (Sharma, column 3, lines 46-60)

Therefore, it would have been obvious to combine the teachings of the Tremblay and Short references with the Sharma reference for the benefit of improving performance as specified in claim 44.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Short (US Patent # 5,633,865) and

Sharma (US Patent # 6,055,605) as applied to claim 44 above, and further in view of Orton et al.(US Patent # 5,379,432).

With respect to claim 45, the Tremblay reference teaches wherein the multiple programmable units comprise multiple units and a programmable processor integrated within the processor. (column 4, lines 7-29, where P2 processor 210 can issue commands as well)

However, the combination of the Tremblay, Short, and Sharma references does not explicitly teach that the programmable processor has a different architecture than the multiple programmable units.

The Orton reference does teach that the programmable processor has a different architecture than the multiple programmable units. (column 13, line 51 to column 14, line 2)

The Tremblay, Short, Sharma, and Orton references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Tremblay, Short, and Sharma references to have the programmable processor to be a different architecture than the multiple programmable units, which is taught by the Orton reference.

The suggestion/motivation for doing so would have been to allow access for processors of different architectures to share the same address space. (Orton, column 13, line 51 to column 14, line 2)

Therefore it would have been obvious to combine the teachings of Tremblay, Short, Sharma, and Orton references for the benefit of shared memory to obtain the invention as specified in claim 45.

2. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 28-45 in the Pre-Appeal Brief Request dated 7/7/09 have been considered but are moot in view of the new ground(s) of rejection. The Examiner has included the Sharma reference to cure the alleged deficiencies of the Tremblay, Short, Orton, and Tran reference.

3. CLOSING COMMENTS

Conclusion

Applicant's amendment [dated 2/10/09] necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 28-45 have received a third action on the merits and are subject of a third action final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasith Thammavong whose telephone number is (571) 270-1040 can normally be reached on Monday - Thursday 9:00am - 6:00pm and the first Friday of the bi-week, 9:00 am –5:00 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571) 272-4190. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Prasith Thammavong/
Patent Examiner
Art Unit 2187
December 17, 2009

/Brian R. Peugh/
Primary Examiner, Art Unit 2187
December 14, 2009